What is claimed is:

1. An array-type processor in which a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, are arranged in rows and columns, and a state control unit causes successive transitions of operating states of the multiplicity of processor elements for each operating cycle by means of contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas;

one said state control unit is connected to the plurality of element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; and

said state control unit temporarily halts operations of said element areas that correspond to a prescribed number of said operating states that are set to one said context during said operating cycles in which said operating states do not occur.

2. An array-type processor in which a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, are arranged in rows and columns, and state control units cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by means of contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas;

each of the plurality of element areas is connected to a respective state control unit of an equal number of the element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; and

said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur.

3. An array-type processor in which a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, are arranged in rows and columns, and state control units cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by means of contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a number ($a \times b$) of element areas;

each of a number (a) of said state control units is connected to a respective group of (b) element areas of these ($a \times b$) element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts;

said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur.

4. An array-type processor according to claim 1, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

5. An array-type processor according to claim 2, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

6. An array-type processor according to claim 3, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

7. An array-type processor according to claim 1, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

8. An array-type processor according to claim 2, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

9. An array-type processor according to claim 3, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

10. An array-type processor according to claim 4, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

11. An array-type processor according to claim 5, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

12. An array-type processor according to claim 6, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.